REMARKS

With regard to the objection of the specification not defining a "GX packet", applicant points out that the GX packet is defined in figure 3a and on page 9 line 11-14: "GX packet 52 comprises a GX header 54 and GX payload 56, and a Frame Check Sequence (FCS) 58." The details of the GX header are described in figure 3b and on page 9 lines 15 - page 10 line 2.

With regard to the claim objection of claims 3 and 68, the word "further" has been removed from these claims.

With regard to the claim objection of claim 10, the antecedent references were to the earlier-defined "data lanes", not a particular data lane number. However, applicant has amended antecedent references "said data lane m", "said data lane 0", and "said data lane 1" by removing the word "said" in these three instances.

With regard to the claim objection of claim 66, applicant has amended the claim according to the examiner's suggestion.

With regard to the 35 USC 112 rejection of claim 1, applicant has amended the claim to properly show the FCS being transmitted after the variable length payload, as

shown in figure 3a and described in the specification on page 9 line 11-14.

With regard to the 35 USC 112 rejection of claim 10, applicant has amended claim 10 to show IDLE transmitted on lanes m+2 through n.

The 35 USC 112 rejections of dependant claims 2-21 and 68-72 are addressed by the amended claims 1 and 66.

With regard to the 35 USC 102 rejection of claims 1-2 and 66-67 over Garcia, applicant points out that Garcia teaches a SONET/SDS header 40 which precedes a fixed length payload 50 or 60. Each datagram of figure 5 is a fixed length, and occupies a particular slot time, such as "slot #1" time, as would be done for a DS-1 synchronous payload. The packet is chopped up to fit into each of these "slot #1" times over multiple SONET frames until the transmission is complete. The presumption made in SONET systems is that there will be negligible packet loss, so the There are three distinguishing features of SONET systems when compared to the present invention:

First, because the ethernet packet is provisioned into a DS0 time slot, the variable length ethernet packet must be chopped up into successive DS0 time slots, each time slot sized at 64 byte pieces. When the ethernet packet is chopped up into these 64 byte pieces, and presented into a specific slot time over multiple successive SONET frames, this creates the need for a new function of "segmentation

and reassembly" (SAR) to break up the the ethernet packet on transmit and reassemble the chopped up ethernet packet on receive, as well as re-delineate the start and end of packet for each packet so treated, which would include the ethernet FCS, as well as detect any lost pieces of the packet during transmission because of loss of SONET/SDM frames. This important SAR function is required when adapting connectionless protocols such as variable length ethernet packets into connection-oriented protocols with fixed time interval cell-based transport such as the SONET/SDM of Garcia. The genesis of SONET/SDH was transporting fixed-length cells carrying voice information slots such as DS0, which is then adapted to carry variable length ethernet packets. Figure 13 of Garcia shows the SAR 138.

A second distinction between SONET systems carrying ethernet and the present invention is the aspect of synchronous clocking. In Garcia, SONET frames are propagated through an entire SONET infrastructure, and clocking information is extracted and used to regenerate the clocks on the output ports. The SONET/SDH header includes a pointer to the start of data, and the balance is taken care of with elasticity buffers. Ethernet frames enter the system and may be at different clocking rates, which would cause buffers to either overflow or run empty. The elasticity buffers required of Garcia are found on 317 of figure 31E. There is no such rate adaptation in the present

invention, and elasticity buffers to compensate for different clocking rates are not present in the present invention.

A third distinction between the SONET system of Garcia and the present invention is that claim 1 of the present invention recites "variable length payload", while the system of Garcia has payloads fixed at 64 bytes, the size of their SONET/SDH cell.

A fourth distinction between the SONET system of Garcia and the present invention is the nature, order, and coverage of FCS (frame check sequences). In SONET/SDH, the header (40 of figure 4) includes an FCS 40 which is transmitted before the payload, and does not operate over the successor payload 50 or 60. In the payloads 50 or 60, the ethernet packet (including FCS) is chopped up and sent over multiple cells, and assembled at the SAR where the FCS is checked. In contrast with the amended claims of the present invention, Garcia does the following (italics added for emphasis):

1) Send SONET/SDH idle sequence (first part of the SONET header) - *same as present application.*

2) Send SONET/SDH header which includes a pointer to the cells that follow and a packet type, along with an FCS that operates only on the header - *the present invention does not have an FCS for the header.*

3) Send multiplexed ethernet packet data from several different sources, where each source is chopped up into 64 byte cells, each cell separately including a header and an FCS for the cell, separate from the FCS of the reconstructed ethernet packet after segmentation and reassembly (SAR). - *the present invention does not chop up the ethernet packet, but rather sends the entire variable length data packet at once, does not multiplex it over successive frames, and there is only one header for the entire ethernet packet, not one for the frame and another one for each chopped-up packet within the frame.*

Reconsideration is requested for the rejections of claims 1, 2, 66, and 67.

With regard to the 35 USC 102 rejection of claims 1 and 66, applicant points out that since the art of Garcia does not teach a system for transmitting variable length data, the combination with Finney does not anticipate the present invention. Finney teaches the splitting of data across a plurality of serial links distinct from the present invention of splitting data into "data lanes", and Finney does not teach the transmission of start of frame or end of frame symbols within those lanes, which is an essential requirement for the transmission of data packets. Finney teaches the transmission of bulk data that has not been packetized across a plurality of serial links, which are

data lanes one bit wide. In the case where Finney is used to transmit ethernet packets, there would be no means of distinguishing delineations from one packet from another, and furthermore, start of packet would occur in any random data lane, and not in a deterministic first lane, as in the present invention. The alignment of the header in the byte lanes is important for the quick recovery of header information, and is not available in Finney. Furthermore, Finney does not disclose sending of data in lanes more than one bit wide. Reconsideration of the 35 USC 103 rejection is requested.

Claim 24 is written as an independant claim which includes the limitations of claims 22 and 23. The fee difference between claim 24 as an independant claim and a dependant claim is enclosed.

Version with markings to show changes made

The following claims are amended as follows:

3 (Amended) the process of claim 2 wherein said header [further] includes declaration fields for at least one of BPDU, PRIORITY, VLAN_ID, and an application specific field.

10 (Amended) the process of claim 9 wherein

said second step comprises transmitting said header across said n data lanes until all said header information has been sent;

said third step comprises transmitting said variable length payload, wherein during a final payload cycle, said payload ends on a [said] data lane m;

for the case where m < n, said fourth step includes sending on said final payload cycle said END symbol on lane m+1, and said IDLE symbol on any available data lanes [m=n+2] m+2 through n;

for the case where m = n, said fourth step comprises sending said END symbol on [said] data lane 0, and said IDLE symbol on [said] data lane 1 through said data lane n.

24 (Amended) A communication interface comprising n data lanes, said interface sequentially transmitting a header distributed across a plurality of said data lanes, a variable amount of payload data distributed across a plurality of said n data lanes;

said header includes transmitting a START symbol on first said data lane, and the transmission of said payload data is followed by an END symbol on at least one said data lane; [The communication interface of claim 23 wherein said transmission of]

said payload data includes transmitting data across said n data lanes up to data lane m, where m <= n.

66 (Amended) A communications interface for sending or receiving a packet, said packet comprising, in sequence, a header, variable length payload, and a terminator;

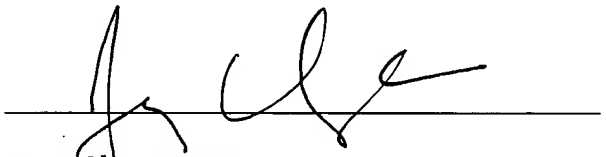
said header including a START symbol and a TYPE field identifying the format of said payload;

said terminator including an END symbol;

wherein said START symbol is transmitted first, followed by the remainder of said header, followed by said variable length packet [data] payload, followed by said terminator.

With this amendment, this application is in condition for allowance. Examiner is advised that agent Chesavage may be reached by telephone at 650-619-5270, or via e-mail at patents@chesavage.com

Respectfully Submitted,



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